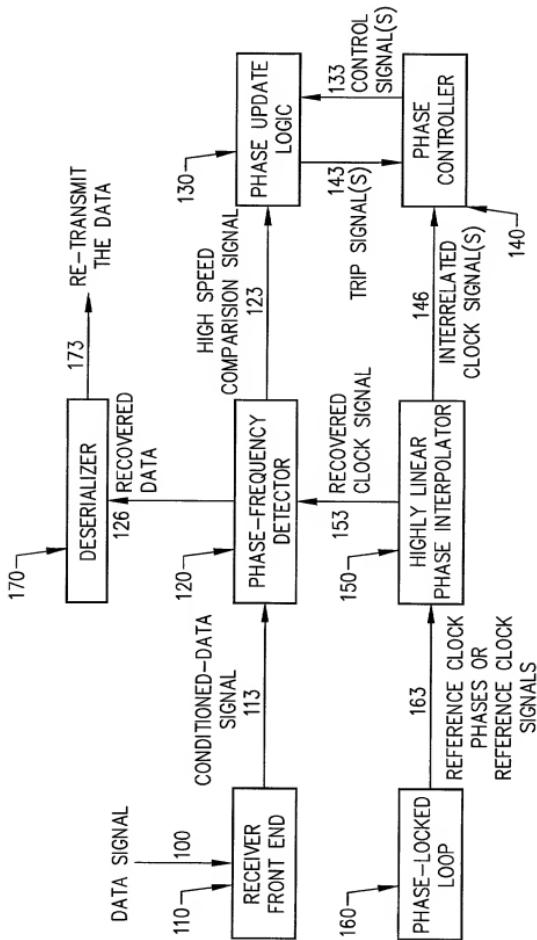


FIGURE 1



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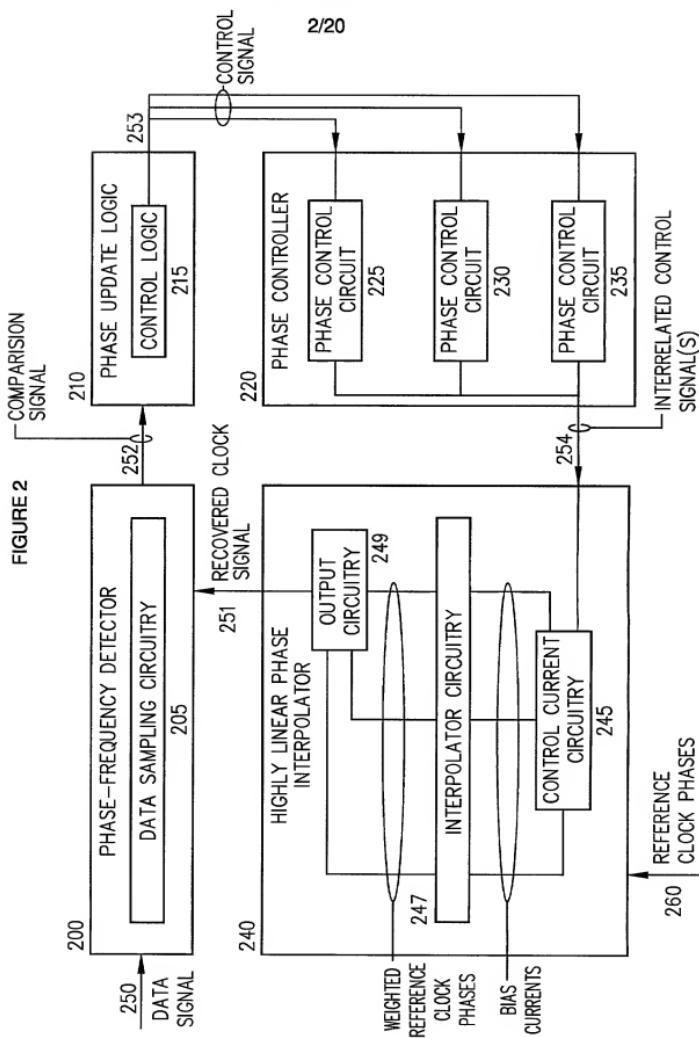


FIGURE 3A

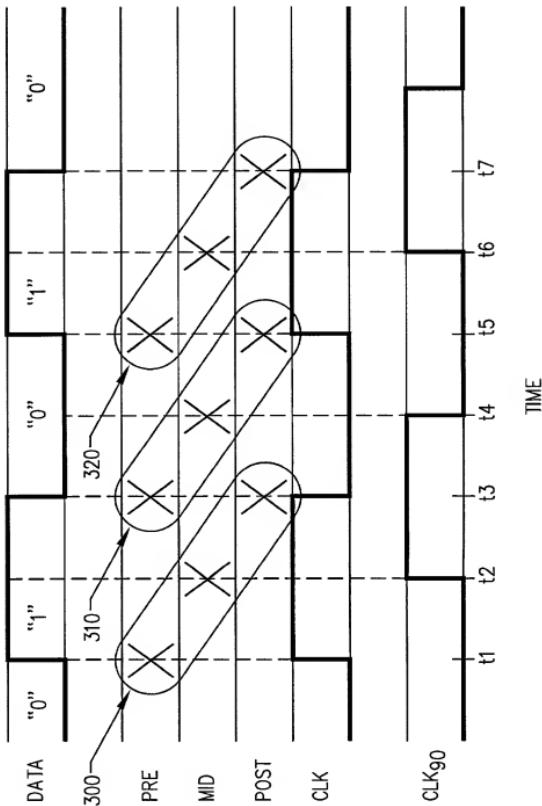
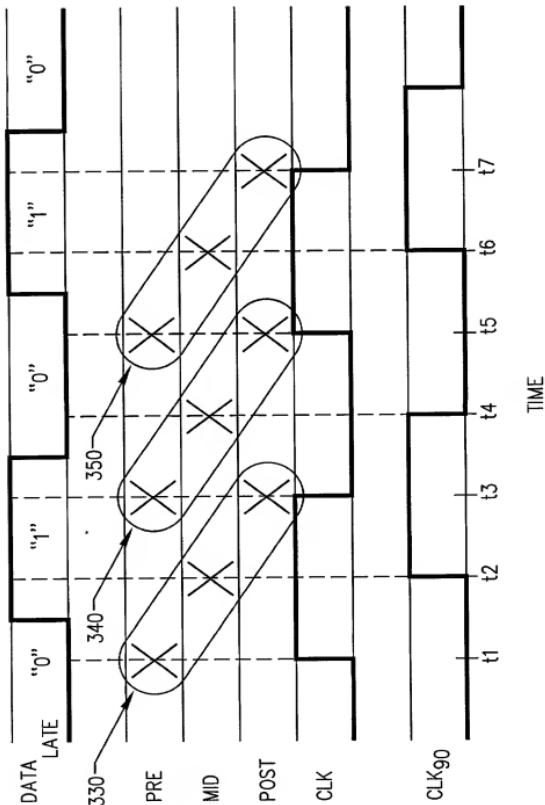


FIGURE 3B

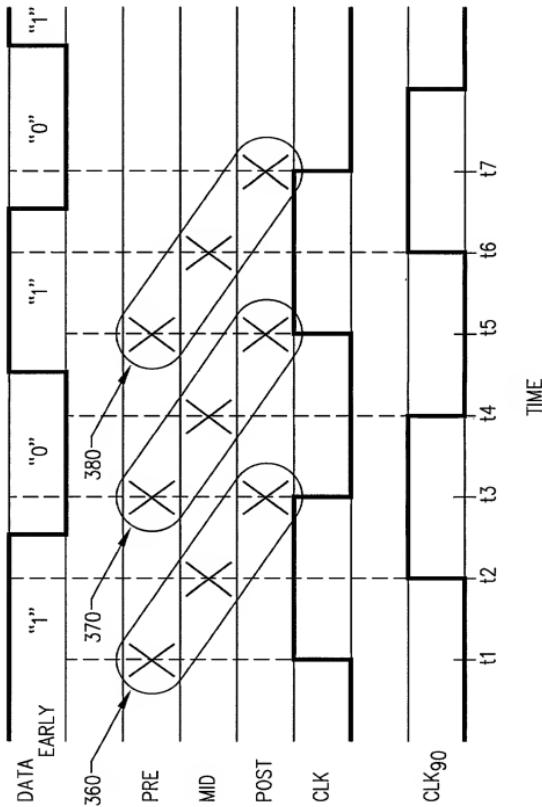


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FIGURE 3C



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FIGURE 4

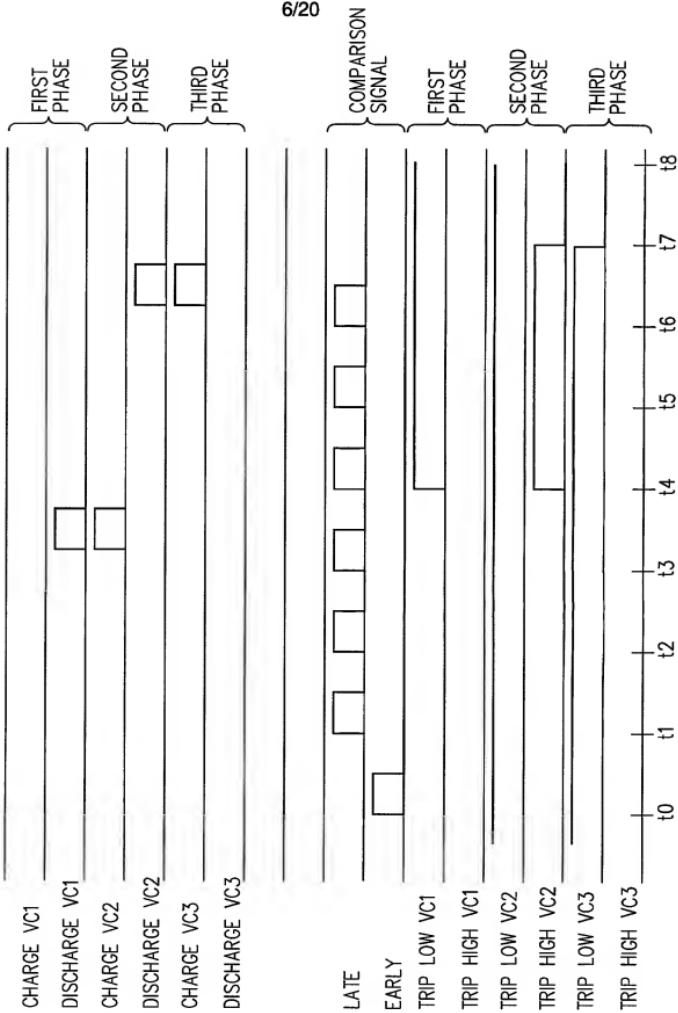
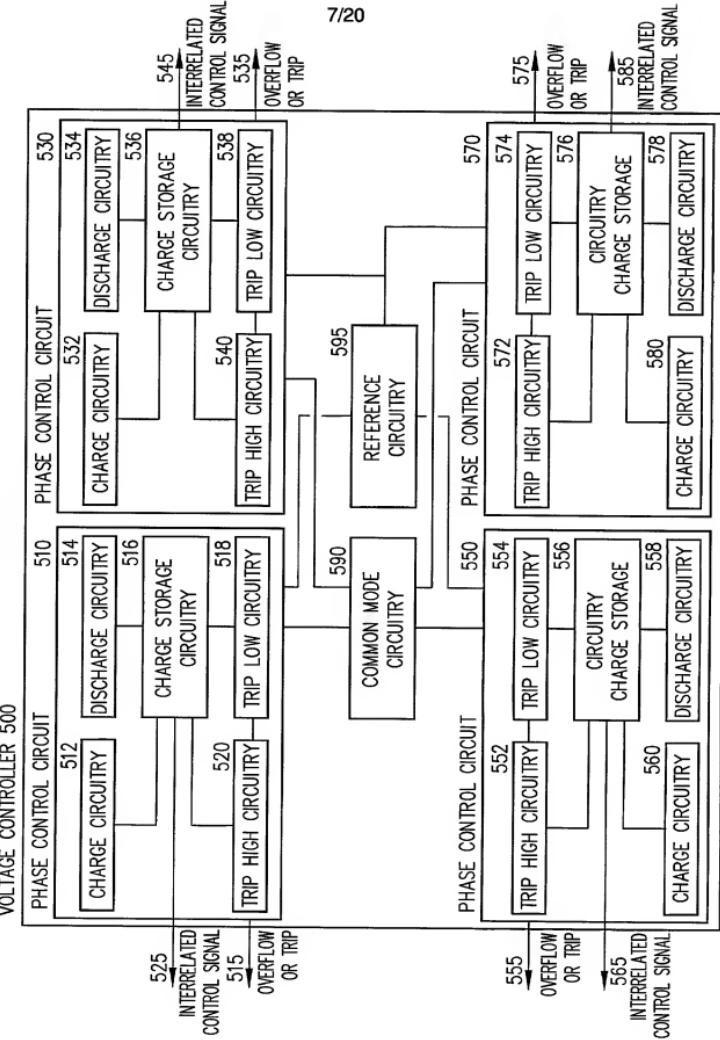


FIGURE 5



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FIGURE 6

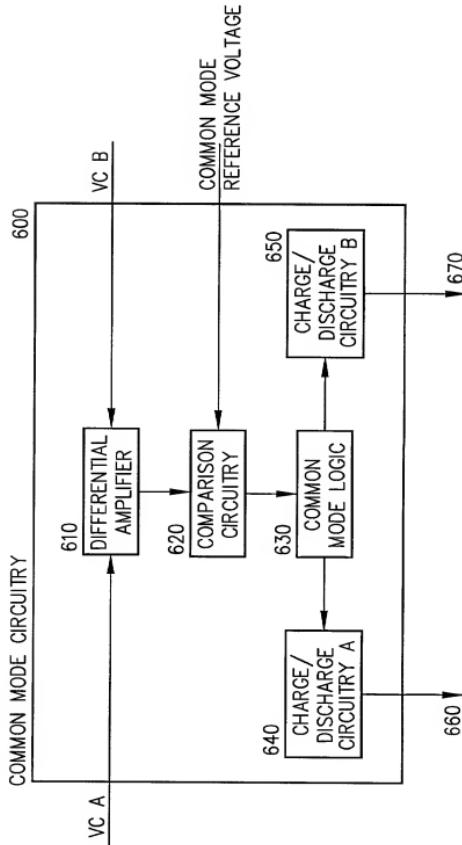
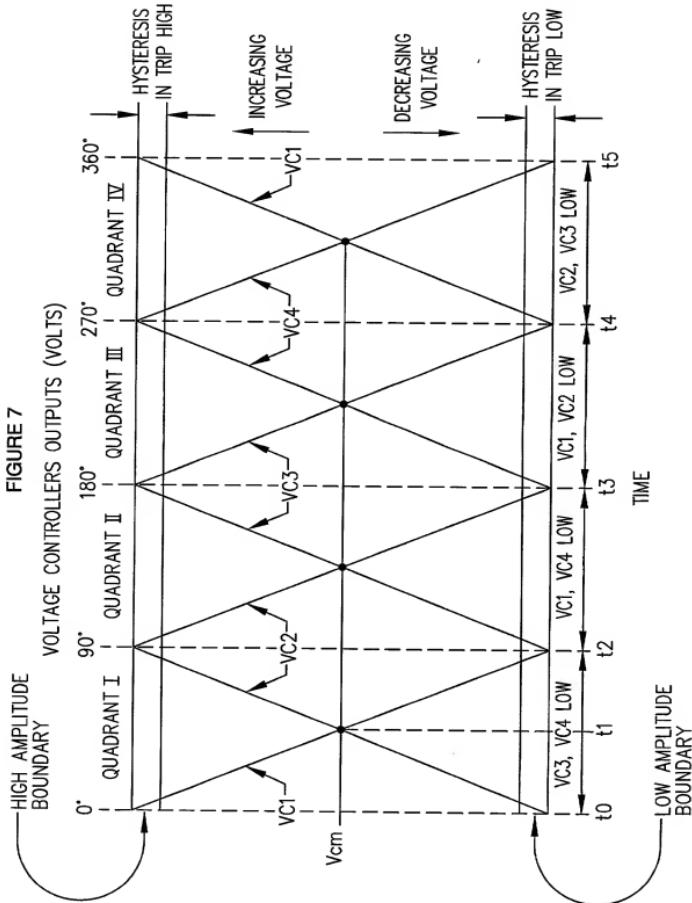
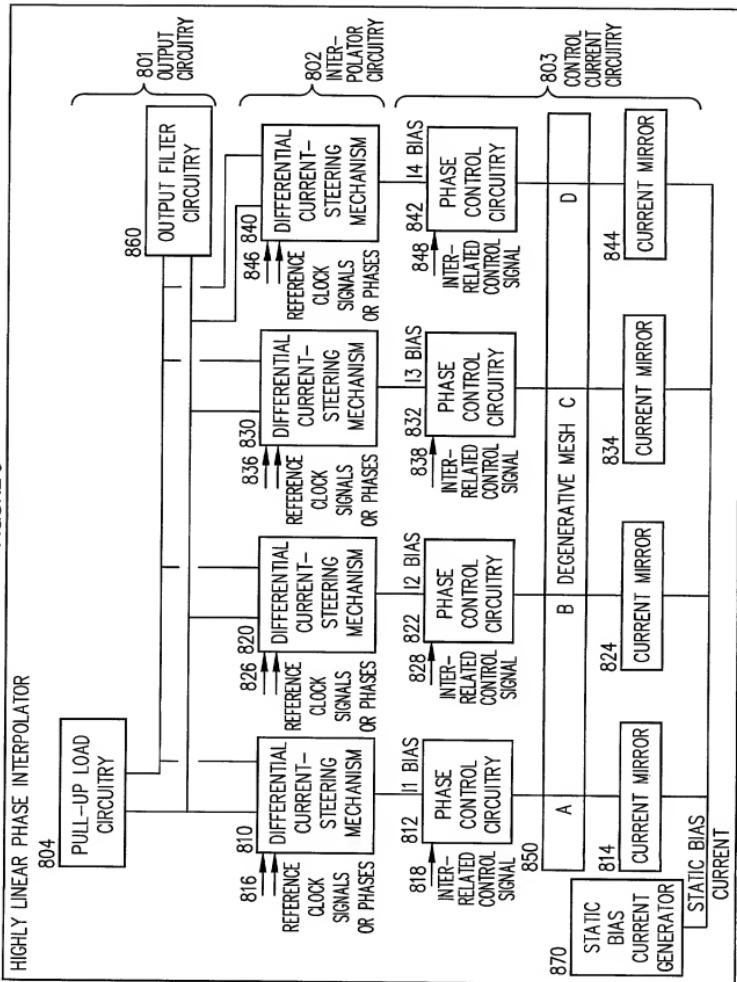


FIGURE 7



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FIGURE 8



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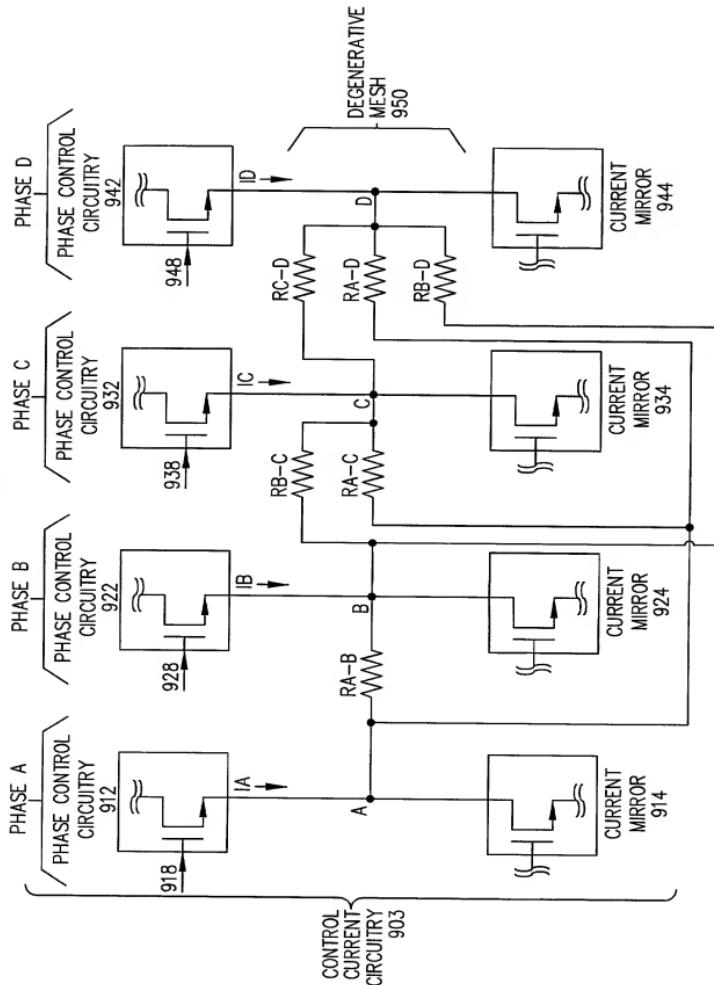
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FIGURE 9



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FIGURE 10

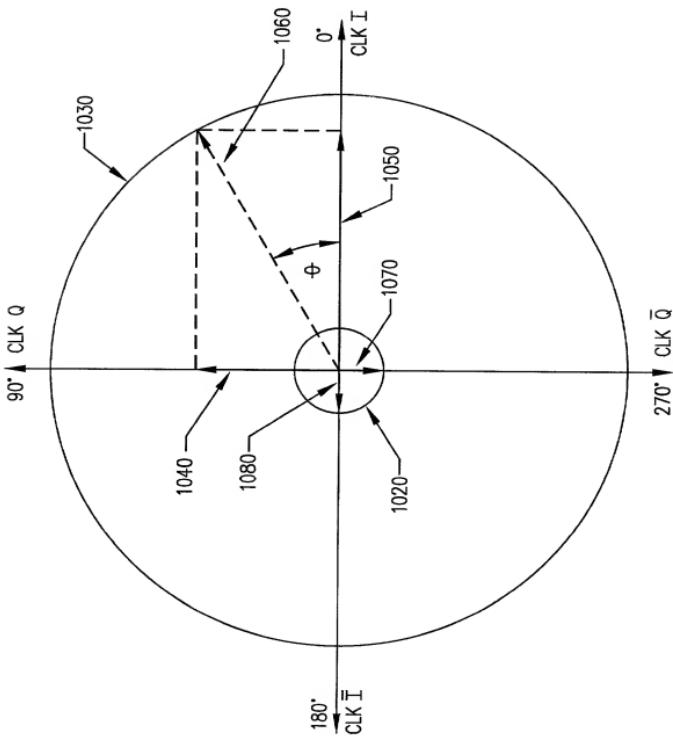
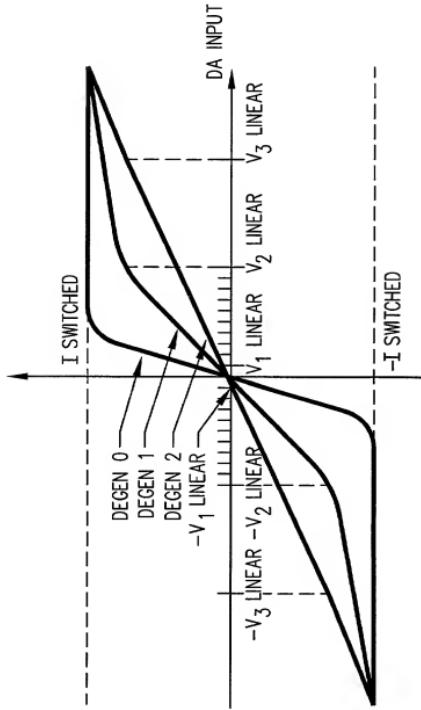


FIGURE 11

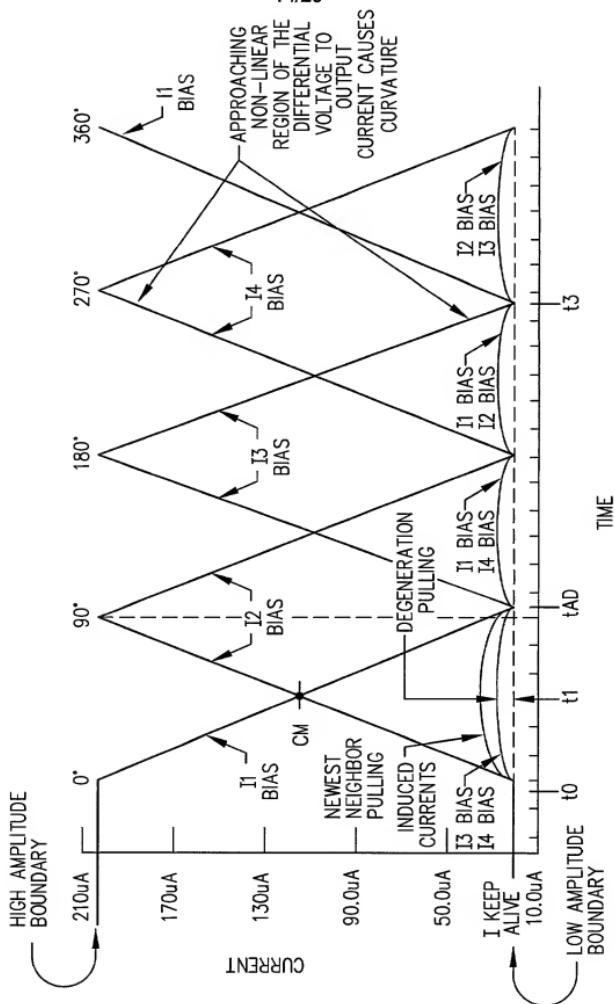
PSEUDO-DIFFERENTIAL AMPLIFIER CURRENT OUTPUT (DA OUT)



PSEUDO-DIFFERENTIAL AMPLIFIER SWING RANGE BASED ON DEGENERATION

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FIGURE 12



1300

RECEIVING A DATA SIGNAL

1310 COMPARING THE DATA SIGNAL TO A RECOVERY CLOCK SIGNAL

1320 DETERMINING AN UPDATE PATTERN TO PROVIDE PHASE UPDATES FOR SAID GENERATING INTERRELATED CONTROL SIGNALS IN THE ABSENCE OF DATA TRANSITIONS

1330 GENERATING A CHARGE AND DISCHARGE SIGNAL BASED UPON SAID COMPARING

1340 GENERATING INTERRELATED CONTROL SIGNALS BASED ON SAID COMPARING

1350 COMBINING AMPLITUDE CONTRIBUTIONS FROM PHASES OF A REFERENCE CLOCK SIGNAL WHEREIN THE AMPLITUDE CONTRIBUTIONS ARE BASED ON THE INTERRELATED CONTROL SIGNALS, TO CHANGE A PHASE OF THE RECOVERED CLOCK SIGNAL WITH AN ANALOG TRANSITION

FIGURE 13

1335

GENERATING A CHARGE SIGNAL TO INCREASE AN AMPLITUDE OF A FIRST INTERRELATED CONTROL SIGNAL OF THE INTERRELATED CONTROL SIGNALS SUBSTANTIALLY SIMULTANEOUSLY WITH GENERATING A DISCHARGE SIGNAL TO DECREASE AN AMPLITUDE OF A SECOND INTERRELATED CONTROL SIGNAL OF THE INTERRELATED CONTROL SIGNALS

1345

GENERATING A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL TO ADJUST THE AMPLITUDE CONTRIBUTIONS FROM A FIRST PHASE AND A SECOND PHASE OF THE PHASES OF THE REFERENCE CLOCK SIGNAL, WHEREIN ADJUSTMENTS TO THE AMPLITUDE CONTRIBUTIONS OF THE FIRST PHASE AND THE SECOND PHASE ARE SUBSTANTIALLY INVERSELY PROPORTIONAL

1350

GENERATING A FIRST RAMPING CONTROL SIGNAL AND A SECOND RAMPING CONTROL SIGNAL, WHEREIN AN AMPLITUDE OF THE FIRST RAMPING CONTROL SIGNAL INCREASES AT A RATE SUBSTANTIALLY EQUIVALENT TO A RATE THAT AN AMPLITUDE OF THE SECOND RAMPING CONTROL SIGNAL DECREASES

1365

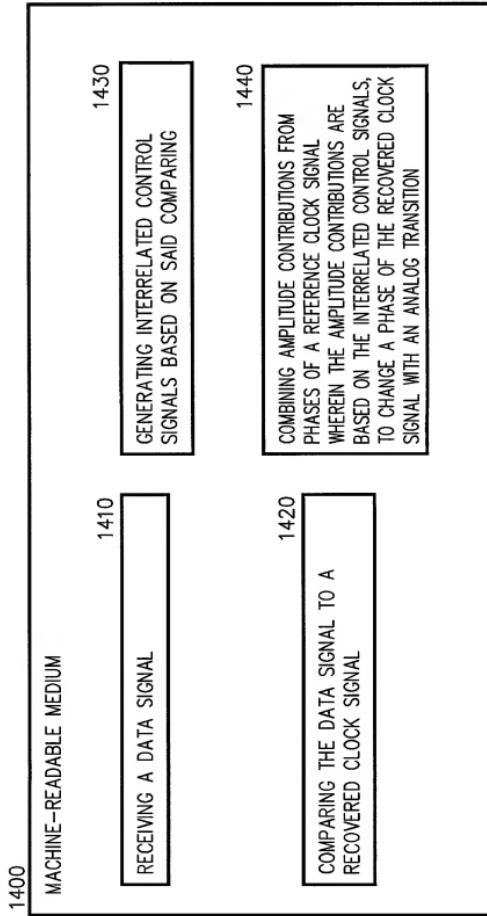
GENERATING DIFFERENTIAL SIGNALS WITH AT LEAST ONE OF THE PHASES OF THE REFERENCED CLOCK SIGNAL, BASED UPON THE INTERRELATED CONTROL SIGNALS, AND FILTERING THE DIFFERENTIAL SIGNALS TO CHANGE THE PHASE OF THE RECOVERED CLOCK SIGNAL WITH THE ANALOG TRANSITION

INTEGRATING THE DIFFERENTIAL SIGNALS

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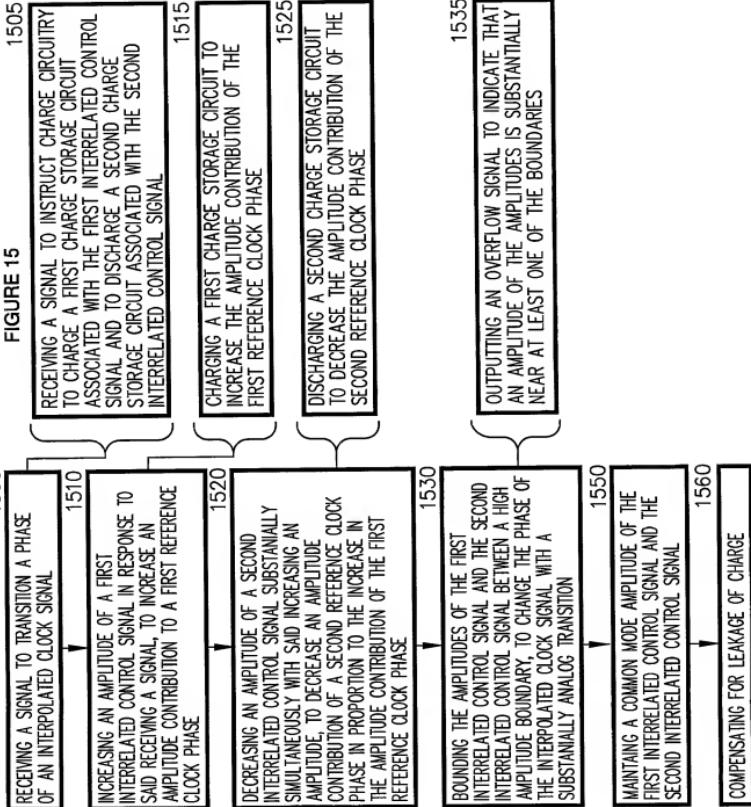
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FIGURE 14



1500

FIGURE 15



1505

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1515

1540
OUTPUTTING AN OVERFLOW SIGNAL BASED ON A HYSTERESIS RANGE OF AMPLITUDES TO PREVENT CHATTER IN THE OVERFLOW SIGNAL

1535

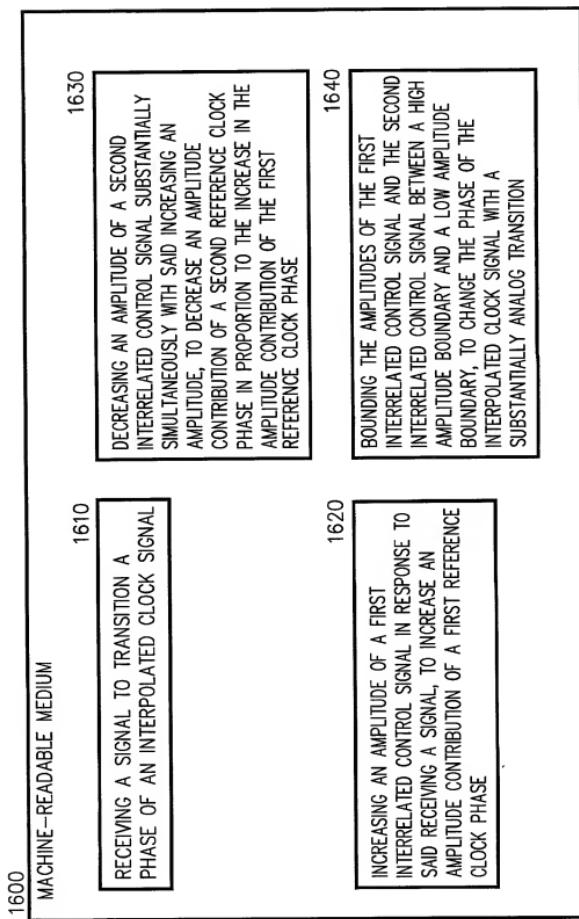
1535
OUTPUTTING AN OVERFLOW SIGNAL TO INDICATE THAT AN AMPLITUDE OF THE AMPLITUDES IS SUBSTANTIALLY NEAR AT LEAST ONE OF THE BOUNDARIES

1550

1550
MAINTAINING A COMMON MODE AMPLITUDE OF THE FIRST INTERRELATED CONTROL SIGNAL AND THE SECOND INTERRELATED CONTROL SIGNAL

1560
COMPENSATING FOR LEAKAGE OF CHARGE

FIGURE 16



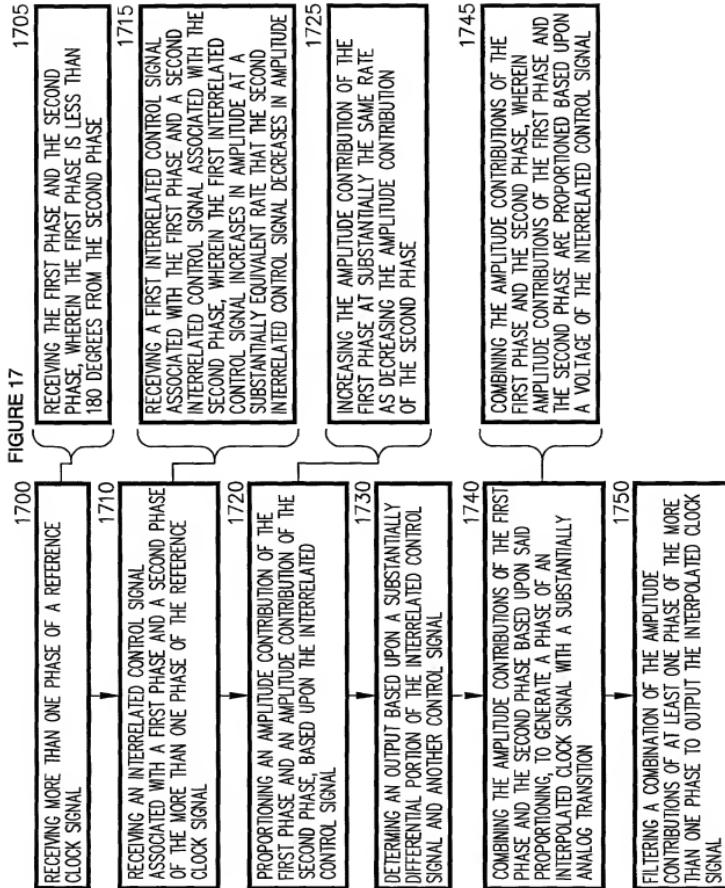


FIGURE 18

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VOLTAGE CONTROLLER FOR A HIGHLY LINEAR PHASE INTERPOLATOR
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